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**1** Compilation techniques for embedded applications: Automatic translation of software binaries onto FPGAs

Gaurav Mittal, David C. Zaretsky, Xiaoyong Tang, P. Banerjee

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(275.28 KB) Additional Information: full citation, abstract, references, index terms

The introduction of advanced FPGA architectures, with built-in DSP support, has given DSP designers a new hardware alternative. By exploiting its inherent parallelism, it is expected that FPGAs can outperform DSP processors. This paper describes the process and considerations for automatically translating binaries targeted for general DSP processors into Register Transfer Level (RTL) VHDL or Verilog code to be mapped onto commercial FPGAs. The Texas Instruments C6000 DSP processor architecture i ...

**Keywords**: binary translation, compiler, decompilation, hardware-software co-design, reconfigurable computing

**2** Design of secure cryptography against the threat of power-attacks in DSP-embedded processors

Catherine H. Gebotys

February 2004 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Issue 1

Full text available: pdf(214.56 KB) Additional Information: full citation, abstract, references, citings, index terms

Embedded wireless devices require secure high-performance cryptography in addition to low-cost and low-energy dissipation. This paper presents for the first time a design methodology for security on a VLIW complex DSP-embedded processor core. Elliptic curve cryptography is used to demonstrate the design for security methodology. Results are verified with real dynamic power measurements and show that compared to previous research a 79% improvement in performance is achieved. Modification o ...

**Keywords**: VLIW

**3** Power analysis and low-power scheduling techniques for embedded DSP software

Mike Tien-Chien Lee, Vivek Tiwari, Sharad Malik, Masahiro Fujita

September 1995 **Proceedings of the 8th international symposium on System synthesis**

Full text available: pdf(208.92 KB) Additional Information: full citation, abstract, references, citings, index terms
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Abstract: This paper describes the application of a measurement based power analysis technique for an embedded DSP processor. An instruction-level power model for the processor has been developed using this technique. Significant points of difference have been observed between this model and the ones developed earlier for some general-purpose commercial microprocessors. In particular, the effect of circuit state on the power cost of an instruction stream is more marked in the case of this DSP pr ...

**Keywords**: DSP processor, application specific integrated circuits, circuit CAD, circuit state, digital signal processing chips, embedded DSP software, energy consumption, energy minimization, energy reduction, general-purpose commercial microprocessors, instruction sets, instruction-level power model, low-power scheduling, measurement based power analysis, micro-architectural power model, on-chip Booth multiplier, power analysis, real-time systems, scheduling, scheduling algorithm

4 Synthesis for Low Power: Current consumption dynamics at instruction and program level for a *VLIW* DSP processor
Radu Muresan, Catherine H. Gebotys
September 2001 **Proceedings of the 14th international symposium on Systems synthesis**

Full text available: pdf(707.88 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a new methodology for analyzing low-level current dynamics at the instruction level and the program level for a VLIW DSP processor core. An efficient methodology for software power analysis is presented which unlike other research supports dynamic current analysis and complex VLIW processor cores. Analysis of high bank register allocation, equivalent functional construct usage, and program-based current, power, and energy is presented. The basic principles and methods develo ...

**Keywords**: DSP processors, current dynamics, methodology

5 Fast, Accurate Static Analysis for Fixed-Point Finite-Precision Effects in DSP Designs
Claire F. Fang, Rob A. Rutenbar, Tsuhan Chen
November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(199.70 KB) Additional Information: full citation, abstract, index terms

Translating digital signal processing (DSP) software intoits finite-precision hardware implementation is often a time-consumingtask. We describe a new static analysis techniquethat can accurately analyze finite-precision effects arisingfrom fixed-point implementations of DSP algorithms.The technique is based on recent interval representation methodsfrom affine arithmetic, and the use of new probabilisticbounds. The resulting numerical error estimates are comparableto detailed statistical simulat ...

6 ClariNet: a noise analysis tool for deep submicron design
Rafi Levy, David Blaauw, Gabi Braca, Aurobindo Dasgupta, Amir Grinshpon, Chanlee Oh, Boaz Orshav, Supamas Sirichotiyakul, Vladimir Zolotov
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(101.67 KB) Additional Information: full citation, abstract, references, citings, index terms

Coupled noise analysis has become a critical issue for deep-submicron, high performance

design. In this paper, we present, ClariNet, an industrial noise analysis tool, which was developed to efficiently analyze large, high performance processor designs. We present the overall approach and tool flow of ClariNet and discuss three critical large-processor design issues which have received limited discussion in the past. First, we present how the driver gates of a coupled interconnect network a ...

**7** Automatic formal verification of DSP software

David W. Currie, Alan J. Hu, Sreeranga Rajan

June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(82.83 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a novel formal verification approach for equivalence checking of small, assembly-language routines for digital signal processors (DSP). By combining control-flow analysis, symbolic simulation, automatic decision procedures, and some domain-specific optimizations, we have built an automatic verification tool that compares structurally similar DSP assembly language routines. We tested our tool on code samples taken from a real application program and discovered several pr ...

**8** Arithmetic: A faster distributed arithmetic architecture for FPGAs

Radhika S. Grover, Weijia Shang, Qiang Li

February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**

Full text available: pdf(379.35 KB) Additional Information: full citation, abstract, references

Distributed Arithmetic (DA) is an important technique to implement digital signal processing (DSP) functions in FPGAs. However, traditional lookup table (LUT) based DA architectures contain one or more carry propagation chains in the critical path that dictates the fastest time at which an entire design can run. In this paper, we describe a novel technique that can reduce or eliminate the carry-propagate chain from the critical path in LUT based DA architectures on FPGAs. In the proposed scheme, ...

**Keywords**: DALUT, XC4000, carry propagation, cost-performance analysis, distributed arithmetic

**9** A constraint driven approach to loop pipelining and register binding

B. Mesman, M. Strik, A. H. Timmer, J. L. van Meerbergen, J. A. G. Jess

February 1998 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(88.00 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Code generation methods for DSP applications are hampered by the combination of tight timing constraints imposed by the performance requirements of DSP algorithms, and resource constraints imposed by a hardware architecture. In this paper, we present a method for register binding and instruction scheduling based on the exploitation and analysis of resource- and timing constraints. The analysis identifies sequencing constraints between operations additional to the precedence constraints. Without ...

**Keywords**: constraint satisfaction, scheduling, register binding, codegeneration, DSP

**10** Testing DSP cores based on self-test programs

W. Zhao, C. Papachristou

February 1998 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(196.83 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

This paper presents a new method for the testing of the datapath of DSP cores based on self-test program. During the test, random patterns are loaded into the core, exercise different components of the core, and then are loaded out of the core for observation under the control of the self-test programs. We propose a systematic approach to generate the self-test program based on two metrics. One is the structural coverage and the other is the testability metric. Experimental results show the self ...

**11** Linear analysis and optimization of stream programs

Andrew A. Lamb, William Thies, Saman Amarasinghe

May 2003 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 2003 conference on Programming language design and implementation**, Volume 38 Issue 5

Full text available: pdf(489.80 KB) Additional Information: full citation, abstract, references, citings, index terms

As more complex DSP algorithms are realized in practice, there is an increasing need for high-level stream abstractions that can be compiled without sacrificing efficiency. Toward this end, we present a set of aggressive optimizations that target linear sections of a stream program. Our input language is StreamIt, which represents programs as a hierarchical graph of autonomous filters. A filter is linear if each of its outputs can be represented as an affine combination of its inputs. Linearity ...

**Keywords**: DSP, FFT, StreamIt, algebraic simplification, embedded, linear systems, optimization, stream programming

**12** A practical approach to static signal electromigration analysis

Nagaraj NS, Frank Cano, Haldun Haznedar, Duane Young

May 1998 **Proceedings of the 35th annual conference on Design automation**

Full text available: pdf(189.87 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

It is commonly thought that sweep-back effects would make electromigration (EM) a non-issue in signal lines. However this is only the case when the shape of the positive and negative current pulses are closely matched. Moreover, as performance pressures increase, the peak current values are exceeding the range for which electromigration models are valid. Thus, during the design of TI's TMS320c6201 DSP chip, it was determined that limits needed to be placed on the current densities in signal ...

**13** System Level Power Modeling and Simulation of High-End Industrial Network-on-Chip

Andrea Bona, Vittorio Zaccaria, Roberto Zafalon

February 2004 **Proceedings of the conference on Design, automation and test in Europe - Volume 3**

Additional Information: full citation, abstract, index terms

Today's System on Chip (SoC) technology can achieve unprecedented computing speed that is shifting the IC design bottleneck from computation capacity to communication bandwidth and flexibility. This paper presents an innovative methodology for automatically generating the energy models of a versatile and parametric on-chip communication IP (STBus). Eventually, those models are linked to a standard SystemC simulator, running at BCA and TLM abstractionlevel. To make the system power simulation fas ...

**Keywords**: Network-on-Chip power analysis, communication based low power design, system-level energy optimization.

**14** Poster abstracts: An algorithm for trading off quantization error with hardware resources for MATLAB based FPGA design
Sanghamitra Roy, Debjit Sinha, Prith Banerjee
February 2004 **Proceedings of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays**
Additional Information: full citation, abstract

Most practical FPGA designs of digital signal processing applications are limited to fixed-point arithmetic owing to the cost and complexity of floating-point hardware. While mapping DSP applications onto FPGAs, a DSP algorithm designer, who often develops his applications in MATLAB, must determine the dynamic range and desired precision of input, intermediate and output signals in a design implementation to ensure that the algorithm fidelity criteria are met. The first step in a flow to map MAT ...

**15** Novel techniques in high-level synthesis: Toward efficient static analysis of finite-precision effects in DSP applications via affine arithmetic modeling
Claire Fang Fang, Rob A. Rutenbar, Markus Püschel, Tsuhan Chen
June 2003 **Proceedings of the 40th conference on Design automation**
Full text available: pdf(146.17 KB) Additional Information: full citation, abstract, references, citings, index terms

We introduce a static error analysis technique, based on smart interval methods from *affine arithmetic*, to help designers translate DSP codes from full-precision floating-point to smaller finite-precision formats. The technique gives results for numerical error estimation comparable to detailed simulation, but achieves speedups of three orders of magnitude by avoiding actual bit-level simulation. We show results for experiments mapping common DSP transform algorithms to implementations us ...

**Keywords**: Static error analysis, affine arithmetic, custom floating-point, embedded hardware, probabilistic error bound

**16** Equivalence verification: Automated equivalence checking of switch level circuits
Simon Jolly, Atanas Parashkevov, Tim McDougall
June 2002 **Proceedings of the 39th conference on Design automation**
Full text available: pdf(220.14 KB) Additional Information: full citation, abstract, references, index terms

A chip that is required to meet strict operating criteria in terms of speed, power, or area is commonly custom designed at the switch level. Traditional techniques for verifying these designs, based on simulation, are expensive in terms of resources and cannot completely guarantee correct operation. Formal verification methods, on the other hand, provide for a complete proof of correctness, and require less effort to setup. This paper presents Motorola's Switch Level Verification (SLV) tool, whi ...

**Keywords**: MOS circuits, VLSI design, custom design, equivalence checking, formal verification, switch level analysis

**17** A hardware/software co-design flow and IP library based on simulink
L. M. Reyneri, F. Cucinotta, A. Serra, L. Lavagno
June 2001 **Proceedings of the 38th conference on Design automation**
Full text available: pdf(119.94 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a design flow for data-dominated embedded systems. We use The

Mathworks' Simulink\trademark environment for functional specification and algorithmic analysis. We developed a library of Simulink blocks, each parameterized by design choices such as implementation (software, analog or digital hardware, \ldots) and numerical accuracy (resolution, S/N ratio). Each block is equipped with empirical models for cost (code size, chip area) and performance (timing, energy), based ...

**18** Hierarchical analysis of power distribution networks

Min Zhao, Rajendran V. Panda, Sachin S. Sapatnekar, Tim Edwards, Rajat Chaudhry, David Blaauw

June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(206.93 KB) Additional Information: full citation, abstract, references, citings, index terms

Careful design and verification of the power distribution network of a chip are of critical importance to ensure its reliable performance. With the increasing number of transistors on a chip, the size of the power network has grown so large as to make the verification task very challenging. The available computational power and memory resources impose limitations on the size of networks that can be analyzed using currently known techniques. Many of today's designs have power network ...

**19** The impact of data characteristics and hardware topology on hardware selection for low power DSP

Gareth Keane, Jonathan Spanier, Roger Woods

August 1998 **Proceedings of the 1998 international symposium on Low power electronics and design**

Full text available: pdf(345.96 KB) Additional Information: full citation, abstract, references, index terms

Adders and multipliers are key operations in DSP systems. The power consumption of adders is well understood but there are few detailed results on the choice of multipliers available. This paper considers how the power consumption of a number of multiplier structures such as Carry-Save array and Wallace Tree multipliers varies with data wordlengths and different layout strategies. In all cases, results were obtained from EPIC PowerMill™ simulations of actual synthesised circuit layout ...

**20** Constraint analysis for DSP code generation

Bart Mesman, Marino T. J. Strik, Adwin H. Timmer, Jef L. van Meerbergen, Jochen A. G. Jess

September 1997 **Proceedings of the 10th international symposium on System synthesis**

Full text available: pdf(966.00 KB) Publisher Site Additional Information: full citation, abstract, references, citings

Code generation methods for DSP applications are hampered by the combination of tight timing constraints imposed by the performance requirements of DSP algorithms, and resource constraints imposed by a hardware architecture. In this paper, we present a method to analyze resource- and timing constraints in a single model. The analysis identifies sequencing constraints between operations additional to the precedence constraints. Without the explicit modeling of these sequencing constraints, a sche ...

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| IEEE CNF | IEEE Conference Proceeding |
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| IEEE STD | IEEE Standard |

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